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SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE

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No. OF CLAIMS 33

This invention relates to an improved semiconductor device and an improved method of manufacturing a semiconductor device. The invention is particularly advantageous in reducing leakage currents in semiconductor diodes and transistors.

Semiconductor diodes and transistors manufactured by the planar method (as disclosed in J.A. Hoerni's U.S. Patent 3,025,589, dated March 20, 1962) offer improved manufacturing yields and enhanced characteristics over other types of semiconductors. In a planar transistor, both the emitter-base and base-collector junction areas at the plane surface of the transistor are limited during fabrication by the use of thermally grown oxide layers or coatings during diffusion. The junctions intersect the semiconductor surface underneath the oxide coating. This non-conducting coating is left on the finished transistor to protect the parts of the junctions that reach the semiconductor surface from contamination and damage during fabrication and for the subsequent life of the transistor.

However, the presence of the oxide coating did not always ensure that leakage currents would be either low or constant. In fact, under certain conditions during fabrication, use, or in high temperature storage, very serious increases in leakage currents have occurred.

The exact cause of the excessive leakage currents is not fully understood. However, it is believed that formation of inversion layers or channels of N-type conductivity on the surface of P-type conductivity transistor r gions, or f rmation of channels of P-typ conductivity on th surfac of N-typ conductivity transistor regions, gr atly influ nce th incr ases in leakage currents.

It is known that the presence of an oxide coating on the surface of a semiconductor body may result in the bending of the energy bands near the surface of the semiconductor. For example, if this bending occurs in a downward direction on a conventional energy band diagram, the Fermi level is removed further from the valence band at the surface of the semiconductor which tends to become more N conductivity type. If the semiconductor body is sufficiently high resistivity P-type, surface inversion will occur to produce an N-type channel.

In a P-N-P transistor, both the emitter and collector surfaces are of P-type conductivity. The collector surface net acceptor concentration normally lies in the range of 10^{15} - 10^{16} atoms per cu.cm., a range in which surface inversion or channel formation is known to occur quite commonly under thermally grown oxides. Since acceptor concentration levels at the low end of this range are required for the fabrication of higher voltage breakdown devices, and since the susceptibility to channel formation increases with decreasing acceptor concentration, it follows that high voltage P-N-P transistors are the most difficult to fabricate without excessive leakage currents due to channel formation being exhibited. Similarly, high voltage N-P diodes are subject to channel formation. Hence, these types of semiconductor devices have exhibited the most serious leakage currents.

Semiconductor devices have also been known to exhibit serious leakage currents due to surface inversion or channelling that occurs on lightly doped semiconductor surfaces under certain ambient conditions. What causes this type of surface channelling is not fully understood.

To my knowledge, there has been no completely

satisfact ry explanation f the cause of the excessive leakage currents, nor has there been a solution for their limination put forward prior to my invention.

It is known, however, that complete removal of a grown oxide coating on a surface of a planar semiconductor device (e.g. by solution in an etchant containing hydrofluoric acid) will remove the surface channels and greatly reduce the leakage currents. However, this procedure offsets some of the advantages of planar type semiconductor devices by exposing the junctions to surface contamination. Furthermore, it does not solve the problem of surface channel formation under certain ambient conditions on other types of semiconductor devices.

I have succeeded in reducing leakage currents in a silicon planar transistor, by a method disclosed in my copending application serial number 846,227 filed April 6, 1962. where first the thermally grown oxide is completely removed and is then replaced with a vacuum evaporated silicon monoxide. This resulted in stable devices entirely free from detectable channels. However, although satisfactorily reducing leakage currents, this method suffered from the disadvantage of requiring an extra fabrication step and also resulted in the temporary exposure of the surface to possible contamination.

Some writers have considered that the increased leakage currents were due to the increase of the effective area of the P-N junction by the area between the channel and the underlying material. I believe, however, that when an N-type channel occurs on the surface of a P-type collector say, it creates an N-type conduction path between th N-typ base and the outer periphery of th semi-

conductor body. Now, the surfaces of semiconductor bodies are usually very carefully prepared and oriented prior to device fabrication to reduce the generation of electron-hole pairs at the surface of the semiconductor. The outer periphery of the semiconductor body, however, is not so carefully prepared. Hence, the many surface defects, cracks, etc. ensure the generation of electron-hole pairs in the faulty crystal lattice at the periphery of the semiconductor body.

Thus, according to my belief, the channel at the interface of the oxide coating and the collector region effectively forms a short-circuit conduction path from the base region to the outer periphery of the semiconductor body and hence to the bottom surface of the collector region. I also believe it is this additional current conduction path caused by the channelling that produces leakage currents when the P-N junction is reverse biased.

I have discovered by ensuring that there is no continuous oxide path left across the surface of the semiconductor body, the leakage currents can be greatly reduced without the necessity of removing the oxide from the parts where the junction extends to the semiconductor surface. In effect, I have rendered the conduction path open circuit by selective removal of the oxide.

According to one aspect of my invention, I provide an improved semiconductor device in which leakage currents are greatly reduced. The device comprises a semiconductor body having a plane surface, the body having a first portion of one conductivity type extending into the body from the surface and a second portion of opposite conductivity type formed by diffusion of an impurity into

part of the first portion from the surface. This defines a r otifying junction between the second portion and the remainder of the first portion that extends to the surface about the second portion. A continuous thermally grown non-conducting coating completely covers the rectifying junction at the surface. According to my invention, an area at the surface completely surrounds the boundary of the junction at the surface in which a band of the coating has been removed to expose the surface.

This is accomplished, in one embodiment of my invention, by forming a non-conducting coating on the plane surface of the first portion in the conventional way. Then an impurity is diffused into a hole opened through the coating to the surface to form the second portion and the junction. A band of the coating is then removed to expose an area of the surface completely surrounding the boundary of the junction at the surface.

Semiconductor surfaces nearly always contain a thin oxide coating due to reaction with oxygen in the air. Therefore, a very thin coating can reform over the area defined by the band. This thin coating should be distinguished from a coating that is formed by a deliberate process of thermal oxidization or deposition.

Because of the presence of this thin oxide coating in the area defined by the band, there is a possibility, under some circumstances, that the disturbing channels can reform after manufacture. This is particularly true of lightly doped semiconductor surfaces which are asily inverted in conductivity type by a comparatively small bending of the nergy bands. Thus, they are subject to chann l reformation due to th presence of the thin

oxid coating which would reestablish a current leakag path across the surfac f the semiconductor. Of course, extreme care in encapsulation of the semiconductor device can minimize the liklihood of channel reformation.

I have discovered, according to another aspect of my invention, that the reoxidized surface of a planar semiconductor device can be rendered insensitive to channelling by diffusing a further impurity into the first portion of the body within the area to form a layer or third portion of the same conductivity type as the first portion. This third portion must have sufficient impurity concentration to prevent the surface within the area from inverting to the conductivity type of the second portion.

It should be readily appreciated by those skilled in the art that this idea of forming a layer or third portion to define an area at the surface completely surrounding the boundary of the junction can be extended to other types of semiconductor devices, such as alloyed types and epitaxial types where surface inversion or channelling has been known to occur under ambient conditions.

Thus, according to another aspect of my invention, I provide an improved semiconductor device comprising a semiconductor body having a first portion of one conductivity type extending into the body from one surface thereof, and a second portion of opposite conductivity type extending into the first portion from the surface. This defines a rectifying junction between the second portion and the remainder of the first portion that extends to the surface about the second portion. A layer or third portion ext nds into a portion of th surface to defin an area at th surfac completely surrounding the boundary of

the junction that extends to the surface. The layer is of the same conductivity type as the first portion and is of sufficient concentration to prevent the surface within the area from inverting to the conductivity type of the second portion.

In the case of planar semiconductor devices, the diffusion of the impurity to form the third portion can be conveniently done at any stage during the manufacture of the device. In the manufacture of diodes, it can be done at a very early stage. For example, as the first step after the non-conducting coating is formed on the surface of the semiconductor body, a band of the coating can be removed to expose an area of the surface and then the impurity can be diffused within the area. For a transistor, where collector leakage currents are to be reduced, I prefer to carry out the diffusion of this impurity concurrently with the emitter diffusion, the impurity being of the same conductivity type and of very high concentration. (In the order of 10^{21} atoms per cu.cm.) For an N-P silicon diode or a P-N-P silicon transistor exhibiting collector leakage currents, the impurity concentration should be at least 10^{17} atoms per cu.cm; but for maximum protection against the reformation of channels, I prefer the impurity concentration to be 10^{18} atoms per cu.cm. or higher. For N-P-N silicon transistors exhibiting base leakage currents, the impurity concentration should be at least 10^{18} atoms per cu.cm.

Preferred embodiments of my invention will now be described, by way of example, with reference to the accompanying drawings where like numbers are used to identify like parts, and in which:

Figures 1, 2, 3, 6, 11, 12, 13, 14, 15, 16, 17, 20, 23, and 25 ar s ctional views through s mic nductor devices at separate stages of manufacture in accordance with various aspects of my invention.

Figures 4, 5, 7, 8, 9, and 10 are sectional views through semiconductor diodes manufactured in accordance with my invention; and

Figures 18, 19, 21, 22, 24, and 26 are sectional views through transistors manufactured in accordance with my invention.

The following description will be made with reference to silicon semiconductor diodes and double diffused silicon transistors of the planar type. However, my invention has application to other types of semiconductors employing different semiconducting materials.

Also, the following description is concerned with the problem of channelling across P conductivity type surfaces which have exhibited the most serious leakage currents across (a) the P surface of N-P diodes; (b) the collector surface of P-N-P transistors; and (c) the base surface of N-P-N transistors. My invention would also have application where leakage currents are caused by surface channelling across N conductivity type surfaces.

Referring to the drawings, Figs. 4, 5, and 7 show semiconductor diodes manufactured according to one aspect of my invention. A semiconductor body shown as a wafer 30 of silicon has a plane surface 31. A first portion 32 of the body 30 includes, for example, an impurity of P conductivity type. A s cond portion or lay r 33 of the b dy is f rmed by the diffusion of an impurity of N c nductivity typ into part f th portion 32 from the

surface 31 to defin a rectifying junction 34 between the portion 33 and the remainder of the portion 32. The junction 34 extends to the surface 31 about the portion 33. A continuous non-conducting coating 35 completely covers the junction 34 at the surface 31. Ohmic contacts 36 and 37 including leads are connected to the portions 33 and 32 respectively. The diode as so far described is substantially the same as the planar diode described in U.S. patent 3,025,589 referred to above. However, according to my invention, an area 38 at the surface 31 in which a band of the coating 35 has been completely removed to expose the surface 31 completely surrounds the boundary of the junction 34 at the surface 31.

Thus, the liklihood that the portion 32, within the area 38 at the surface 31, will invert to form an N conductivity type channel has been greatly minimized. Even when heavy surface channelling is shown to exist at the rest of the surface of the portion 32 under the coating 35, the semiconductor diodes, according to my invention, exhibit very low leakage currents.

In the diode shown in Fig. 7, the surface area 38 extends to the periphery of the portion 32. This provides the additional advantage of reducing collector contact resistance.

In the diode shown in Fig. 5, the contact 36 is located inside the junction 34 on the surface 31 and the contact 37 within the area 38. The area 38 has its innermost edge inside the contact 37. In the diodes shown in Figs. 4 and 7, the contact 37 is located on the opposite surfac 39 f the body 30.

Th methods for making th di des of Figs. 4, 5,

and 7 will n w be described:

Example I

First, the non-conducting coating 35 is formed on a plane surface 31 of the portion 32. (Fig.1). The coating 35 comprises a silicon oxide which can be applied to the surface 31 in a conventional manner such as by the utilization of an oxidizing agent, e.g. by exposure to oxygen or water vapour at elevated temperatures. However, it has become more common to thermally grow silicon dioxide on the surface. Next an impurity is diffused into a hole 40 opened through the coating 35 to expose the surface 31. The diffusion of the impurity forms the portion 33 and the junction 34. (Fig.2). During the diffusion of the impurity into the surface 31, the silicon surface reoxidizes to produce an oxide layer 41 completely covering the surface 31 within the hole 40. A band of the coating 35 is then removed by etching with hydrofluoric acid to expose the area 38 at the surface 31 completely surrounding the boundary of the junction 34. (Fig.3). Faults in the surface of the silicon could create additional conduction paths for leakage currents. Therefore, I prefer to remove the band of the coating 35 as close to the edge of the depletion layer of the junction 34 as practicable.

Alternatively, the removed band may extend to the periphery of the portion 32 as shown in Fig. 6. The contact 36 is then attached to the portion 33 through a hole 42 opened through the coating 41. For the diode of Fig. 4, th contact 37 is attached to the surfac 39. In the diod of Fig. 5, the contact 37 is attach d to the surface 31 within area 38. Car must b taken in attaching the contact 37 to ensur that th innermost edge of the

area 38 is inside the contact. Otherwise a conduction path would remain between the portion 33 and the contact 37 via the channel underneath the coating 35.

Figs.18 and 19 show P-N-P transistors manufactured according to one aspect of my invention. The portions 32 and 33 serve as collector and base portions respectively with the junction 34 serving as the base-collector junction. An emitter portion 43 is formed by the diffusion of an impurity of P conductivity type into part of the base portion 33 from the surface 31 to define an emitter-base junction 44 between the emitter portion 43 and the remainder of the base portion 33. The junction 44 extends to the surface 31 about the emitter portion 43. The non-conducting coating 35 completely covers the junctions 34 and 44 at the surface 31.

According to my invention, the area 38 at the surface 31 completely surrounds the boundary of the junction 34. Emitter, collector and base ohmic contacts 36, 37, and 45 respectively are connected to the emitter portion 43, collector portion 32 and base portion 33.

In the transistor of Fig.18, the emitter and base contacts 36 and 45 are located inside the junctions 44 and 34 respectively on the surface 31, while the collector contact 37 is located on the surface 39. In the transistor of Fig.19, all three contacts 36, 37, and 45 are located on the surface 31, with the area 38 having its innermost edge inside the contact 37.

The transistors of Figs. 18 and 19 are suitable for reducing collector leakage currents which occur most frequently in P-N-P transistors. However, leakage currents can also occur due to an inversion on the surface of the base portion, particularly in N-P-N transistors. Accordingly, Fig.24 shows another embodiment of my invention wherein the area 38 is

located inside the base portion 33 at the surface 31. The base contact 45 is again located inside the base-collector junction 34, with the area 38 having its innermost edge lying inside and its outermost edge lying outside the base contact 45. The collector contact 37 may be attached to the surface 31 through a hole opened through the coating 35.

The methods for making the transistors of Figs. 18, 19, and 24 will now be described.

Example II

As in the case of the diodes, the non-conducting coating 35 is formed on the plane surface 31 of the collector portion 32 (Fig. 1). The base portion 33 is formed as described above with respect to Fig. 2. Next, an impurity is diffused into a hole 46 opened through the coating 41 to the surface 31 to form the emitter portion 43 which defines the emitter-base junction 44. (Fig. 16). During the diffusion, the silicon surface reoxidizes to produce an oxide layer 47 completely covering the surface 31 within the hole 46. A band of the coating 35 is then removed (Fig. 17) to expose the area 38 of the surface 31 completely surrounding the boundary of the junction 34 in the case of the fabrication of the transistors of Figs. 18 and 19. Again, if desired, the removed band may extend to the periphery of the collector portion 32. In the fabrication of transistors of Fig. 24, the band is removed from the base portion 33 as shown in Fig. 23.

In the transistor of Fig. 18, the collector contact 37 is attached to the surface 39. In the transistor of Fig. 19, the collector contact 37 is attached to the surface 31 within the area 38. Care must be taken in attaching the contact 37 to ensure that the innermost edge

of the area 38 lies inside the contact for the same reasons given above. In the transistor of Fig. 24, the collector contact 37 is attached to the surface 31 through a hole 48 opened through the coating 35. In the transistors of Figs. 18, 19, and 24, the emitter contact 36 is attached to the surface 31 through a hole 49 opened through the coating 47. In the transistors of Figs. 18 and 19, the base contact 45 is attached to the surface 31 through a hole 50 opened through the coating 41. In the transistor of Fig. 24, the base contact 45 is attached to the surface 31 within the area 38. Care must be taken to ensure that the innermost edge of the area 38 lies inside and the outermost edge of the area 38 lies outside the contact 45. This is because leakage currents can flow between both junctions 34 and 44 in the case of surface channelling in a base portion.

Figs. 8, 9, and 10 show semiconductor N-P diodes manufactured according to another aspect of my invention. A layer or portion 51 extends into a portion of the surface 31 to define an area 38(a) at the surface 31 completely surrounding the boundary of the junction 34 that extends to the surface 31. The layer 51 is of the same conductivity type as the portion 32. The layer 51 must have sufficient impurity concentration to prevent the surface within the area 38(a) from inverting to N conductivity type. For silicon planar diodes the layer 51 is formed by the diffusion of an impurity into the body 32 from the surface 31 within the area 38. In the diodes of Figs. 8, and 10 the contact 36 is located on the surface 31 and the contact 37 is located n th surface 39 as described with reference to Figs. 4, and 7. Similarly, in Fig. 9, the contacts 36 and 37 are b th loc ted on th surface 31 as described with

reference to Fig. 5. In the diode of Fig. 10, the layer 51 extends to the p riphery of the body 32. The methods for making the diodes of Figs. 8, 9, and 10 will now be described:

Example III

After the method step shown in Fig. 3 for making the diodes of Figs. 4 and 5, a further impurity is then diffused into the body 32 from the surface 31 within the area 38 to form the layer 51. (Fig.13). During the diffusion, an oxide coating 52 reforms within the area 38 to cover the layer 51. It will be noted in the case of Fig. 9, that the innermost edge of the layer 51 lies inside the contact 37.

For an N-P planar silicon diode, the net acceptor concentration of the impurity used to form the layer 51 should be at least 10^{17} atoms per cu.cm. and preferably 10^{18} atoms per cu.cm. or higher.

Thus, the reoxidized surface 52 of the diodes, according to my invention, are rendered insensitive to channelling due to the presence of the layer 51. This is true, even when testing shows that heavy channelling continues to exist on the rest of the surface 31 in the portion 32 under the coating 35.

Example IV

The diodes of Figs. 8, 9, and 10 can also be made by proceeding to the step shown in Fig. 11 after having applied the coating 35 to the surface 31. (Fig.1). First, the band of the coating 35 is removed to expose the area 38 of the surface 31. Then the layer 51 is formed as shown in Fig. 12 by diffusing an impurity into th portion 32 from the surface 31 within the area 38. It can be seen that th area 38(a) now sxtends beyond th area 38 under the

original coating 35. As before, the coating 52 is r formed within the area 38. Thereafter, the portion 33 is formed by diffusing an impurity into the hole 40 opened through the coating 35 as previously explained. (Fig.13). Contacts can then be applied to the diodes as shown in Figs. 8, 9, and 10. Again, if desirable, the layer 51 can extend to the periphery of the body 32. (Fig.14). When diffusing the impurity to form the portion 33, care should be taken to ensure that the boundary of the junction 34 at the surface 31 is completely surrounded by the layer 51.

Figs. 21 and 22 show P-N-P transistors and Fig. 26 shows an N-P-N transistor manufactured according to my invention. In Figs. 21 and 22 the layer or portion 51 is diffused into the collector portion 32 which makes the transistor suitable for reducing collector leakage currents, whereas in Fig. 26 layer 51 is diffused into the base portion 33 which makes the transistor suitable for reducing base leakage currents.

The various methods, according to my invention, for making the transistors of Figs. 21, 22, and 26 will now be described:

Example V

After the steps shown in Figs. 1, 2, 16, and 17 described with reference to Example 2, the layer 51 is formed by diffusing an impurity into the area 38. (Fig.20). The contacts 36, 37, and 45 are then applied as shown in Figs. 21 or 22. It will be noted that the layer 51 has its innermost edge lying inside the collector contact 37 in the case of Fig. 22.

Exampl VI

After the steps of Figs. 1 and 2, the band of th

coating 35 is removed to xpose the area 38, the hole 46 is opened through the coating 41 and the layer 51 is formed simultaneously with the formation of the emitter portion 43. For a P-N-P transistor exhibiting collector leakage currents the impurity used for emitter diffusion is very suitable for forming the layer 51 since it is of the same conductivity type as the collector portion 32 and is of very high concentration (in the order of 10^{21} atoms per cu. cm.). The contacts 36, 37, and 45 can then be applied as shown in Figs. 21 and 22.

Example VII

In an N-P-N transistor exhibiting base leakage currents, the layer 51 is diffused into the base portion 33 as shown in Figs. 23 and 25. Otherwise, the method steps follow the pattern described in Example 5. The finished transistor is shown in Fig. 26. It can be seen that the layer 51 has its innermost edge lying inside and its outermost edge lying outside the base contact 45.

The semiconductor devices of my invention have been shown to greatly reduce undesirable leakage currents caused by surface channelling in semiconductor devices. In the case of surface channelling caused by the presence of an oxide coating on the surface of the planar type semiconductor devices, the advantages of protecting the junctions at all times are maintained. In addition, my invention is applicable to other types of semiconductor devices where surface channelling may be caused by ambient conditions.

Even in cas s wh re it can b shown that surfac channels do exist on the high resistivity P-conductivity type r gion of a semi-conductor device fabricated according

to my invention, such devices do not exhibit undesirable leakage current characteristics normally associated with surface inversion channels. Indeed, since it is well known that surface channels on the high resistivity side of a P-N junction tend to minimize surface breakdown, it may be advantageous to fabricate the semiconductor device under conditions whereby surface channels are intentionally induced. This would ensure bulk breakdown of the junction rather than surface breakdown while at the same time keeping surface leakage currents due to such channelling at a minimum. As is well known, this can be readily accomplished, for example, by heating the finished semiconductor device in the presence of water vapour.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A semiconductor device comprising a semiconductor body having a first portion of one conductivity type extending into said body from one surface thereof, a second portion of opposite conductivity type to said one conductivity type extending into the first portion from said surface to define a rectifying junction between the second portion and the remainder of the first portion, with said junction extending to said surface about the second portion, and a third portion of the same conductivity type as the first portion, the third portion extending into the first portion from said surface to define an area at said surface completely surrounding the boundary of said junction that extends to said surface, the third portion having sufficient impurity concentration of said one conductivity type to prevent said surface within the area from inverting to said opposite conductivity type.

2. A semiconductor diode comprising a semiconductor body of one conductivity type having a layer of opposite conductivity type to said one conductivity type extending into a surface of said body to define a rectifying junction between the layer and the remainder of said body, with said junction extending to said surface about the layer, a further layer of the same conductivity type as said body, the further layer extending into said body from said surface to define an area at said surface completely surrounding the boundary of said junction that extends to said surfac , the further lay r having sufficient impurity concentration of said one conductivity typ to prevent said

surface within the area from inverting to said pp site conductivity type, and ohmic contacts connected to the first mentioned layer and to said body.

3. A semiconductor device comprising a semiconductor body having a plane surface, said body having a first portion of one conductivity type extending into said body from said surface, a second portion of opposite conductivity type to said one conductivity type formed by the diffusion of an impurity into part of the first portion from said surface to define a rectifying junction between the second portion and the remainder of the first portion, with said junction extending to said surface about the second portion, a continuous non-conducting coating completely covering said junction at said surface, an area at said surface completely surrounding the boundary of said junction at said surface in which a band of said coating has been removed to expose said surface.

4. A semiconductor diode comprising a semiconductor body of one conductivity type having a plane surface, said body having a layer of opposite conductivity type to said one conductivity type formed by the diffusion of an impurity into part of said body from said surface to define a rectifying junction between the layer and the remainder of said body, with said junction extending to said surface about the layer, a continuous non-conducting coating completely covering said junction at said surface, an area at said surface completely surrounding the boundary of said junction at said surfac in which a band of said coating has b en removed to expose said surfac , and ohmic contacts connected to the layer and said body.

5. A diode as defined in claim 2 or 4 wherein the area ext nds to the periphery of said body.

6. A diode as defined in claim 2 or 4 wherein one ohmic contact is located inside said junction on said surface, and the other ohmic contact is located in said body on said surface, the area having its innermost edge lying inside said other contact.

7. A diode as defined in claim 2 or 4 wherein one ohmic contact is located inside said junction on said surface, and the other ohmic contact is located on the opposite surface of said body to said one surface.

8. A diode as defined in claim 4 including a further layer of the same conductivity type as said body, formed by the diffusion of an impurity into said body from said surface within said area beneath said coating, the further layer having sufficient impurity concentration of said one conductivity type to prevent said surface within the area from inverting to said opposite conductivity type, and wherein one ohmic contact is located inside said junction on said surface, and the other ohmic contact is located in said body on said surface, the further layer having its innermost edge lying inside said other contact.

9. A transistor comprising a semiconductor body of one conductivity type, a base portion of opposite conductivity type to said one conductivity type extending into a surface of said body to define a base-collector junction between the base portion and the remainder of said body, with the bas -collector junction extending to said surface about the bas portion, an emitter p rtion of said on

conductivity type extending into the base portion from said surface to define an emitter-base junction between th mitter portion and the remainder of the base porti n, with the emitter-base junction extending to said surface about th emitter portion, a further portion of said one conductivity type extending into said body from said surface to define an area at said surface completely surrounding the boundary of the base-collector junction that extends to said surface, the further portion having sufficient impurity concentration of said one conductivity type to prevent said surface within the area from inverting to said opposite conductivity type, and emitter, base and collector ohmic contacts connected to the emitter portion, base portion and said body respectively.

10. A transistor comprising a semiconductor body of one conductivity type, a base portion of opposite conductivity type to said one conductivity type extending into said body from said surface to define a base-collector junction between the base portion and the remainder of said body, with the base-collector junction extending to said surface about the base portion, an emitter portion of said one conductivity type extending into the base portion from said surface to define an emitter-base junction between the emitter portion and the remainder of the base portion, with the emitter-base junction extending to said surface about the emitter portion, a further portion of said opposite conductivity type extending into the base portion from said surface t define an area at said surface completely surrounding the boundary of the emitter-base junction that extends to said surface, the further p rtion having sufficient impurity concentration of said opposite

conductivity type to prevent said surface within the area from inverting to said one conductivity type, and emitter base and collector contacts connected to the emitter portion, base portion and said body respectively.

11. A transistor comprising a semiconductor body of one conductivity type having a plane surface, a base portion of opposite conductivity type to said one conductivity type formed by the diffusion of an impurity into part of said surface to define a base-collector junction between the base portion and the remainder of said body, with the base-collector junction extending to said surface about the base portion, an emitter portion of said one conductivity type formed by the diffusion of an impurity into part of the base portion from said surface to define an emitter-base junction between the emitter portion and the remainder of the base portion, with the emitter-base junction extending to said surface about the emitter portion, a non-conducting coating completely covering the base-collector and emitter-base junctions at said surface, an area at said surface completely surrounding the boundary of the base-collector junction at said surface in which a band of said coating has been removed to expose said surface, and emitter, base and collector ohmic contacts connected to the emitter portion, base portion and said body respectively.

12. A transistor as defined in claim 9 or 11 wherein said area extends to the periphery of said body.

13. A transistor as defined in claim 9 or 11 wher in the emitter contact is located insid the emitter-base junction on said surface, th base c ntact is located inside

the base-collector junction on said surface, and the collector contact is located in said body on said surface, the area having its innermost edge lying inside the collector contact.

14. A transistor as defined in claim 9 or 11 wherein the emitter contact is located inside the emitter-base junction on said surface, the base contact is located inside the base-collector junction on said surface, and the collector contact is located on the opposite surface of said body to said one surface.

15. A transistor as defined in claim 10 wherein the emitter contact is located inside the emitter-base junction on said surface, and the base contact is located within the area on said surface, the area having its innermost edge lying inside and its outermost edge lying outside the base contact.

16. A transistor as defined in claim 11 including a further portion of said one conductivity type formed by the diffusion of an impurity into said body from said surface within the area beneath said coating, the further portion having sufficient impurity concentration of said one conductivity type to prevent said surface within the area from inverting to said opposite conductivity type, and wherein the emitter contact is located inside the emitter-base junction on said surface, the base contact is located inside the base-collector junction on said surface, and the collector contact is located in said body on said surface, the further portion having its innermost edge lying inside the collector contact.

17. A transistor comprising a semiconductor body of one conductivity type having a plane surface, a base portion of opposite c nductivity type to said on conductivity type formed by the diffusion of an impurity into part of said body from said surface to define a base-collector junction between the base portion and the remainder of said body, with the base-collector junction extending to said surface about the base portion, an emitter portion of said one conductivity type formed by the diffusion of an impurity into part of the base portion from said surface to define an emitter-base junction between the emitter portion and the remainder of the base portion, with the emitter-base junction extending to said surface about the emitter portion, a non-conducting coating completely covering the base-collector and emitter-base junctions at said surface, an area at said surface within the base portion completely surrounding the boundary of the emitter-base junction at said surface in which a band of said coating has been removed to expose said surface, and emitter, base and collector ohmic contacts connected to the emitter portion, base portion and said body respectively, the base contact being located within the area on said surface, the area having its innermost edge lying inside and its outermost edge lying outside the base contact.

18. A transistor as defined in claim 17 including a further portion of said opposite conductivity type formed by the diffusion of an impurity into the base portion from said surface within the area beneath said coating the further portion having sufficient impurity concentration of said opposit conductivity type to prevent said surface within the area from inverting to said on conductivity

type the further portion having its innermost edge lying inside and its outermost edge lying outside the base contact.

19. A method for making a semiconductor device comprising the steps of:

(a) forming a non-conducting coating on a plane surface of a first portion of a semiconductor body of one conductivity type;

(b) diffusing an impurity into a hole opened through said coating to said surface within the first portion to form a second portion of opposite conductivity type to said one conductivity type defining a rectifying junction between the second portion and the remainder of the first portion, with said junction extending to said surface underneath said coating about the second portion;

(c) and removing a band of said coating to expose an area of said surface completely surrounding the boundary of said junction at said surface.

20. A method of making a semiconductor diode comprising the steps of:

(a) forming a non-conducting coating on a plane surface of a semiconductor body of one conductivity type;

(b) diffusing an impurity into a hole opened through said coating to said surface to form a layer of opposite conductivity type to said one conductivity type defining a rectifying junction between th layer and the remainder of said body with said junction extending to said surface undern ath said coating about th layer;

(c) removing a band of said coating to expose an area of said surface completely surrounding the boundary of said junction at said surface;

(d) and attaching ohmic contacts to the layer and said body.

21. A method as defined in claim 20 wherein the area extends to the periphery of said body.

22. A method as defined in claim 20 wherein a non-conducting coating is reformed on said surface within said hole, one ohmic contact being attached to said layer through a hole opened through said reformed coating to said surface and the other ohmic contact is attached to the opposite surface of said body to said one surface.

23. A method as defined in claim 20 wherein a non-conducting coating is reformed on said surface within said hole, one ohmic contact being attached to said layer through a hole opened through said reformed coating to said surface, and the other ohmic contact is attached to said surface within the area, the area having its innermost edge lying inside said other contact.

24. A method as defined in claim 20 comprising the further steps of:

(e) reforming a non-conducting coating on said surface within said hole;

(f) diffusing a further impurity into said body from said surface within the area to form a further layer of the same conductivity type as said body, the further layer having sufficient impurity concentration to prevent said surface within th area from inverting to said opposite

conductivity type, one ohmic contact being attached to th first mentioned layer into a hole opened through said reformed coating to said surface, and the other ohmic contact being attached to said surface within the area, the further layer having its innermost edge lying inside said other contact.

25. A method for making a semiconductor device comprising the steps of:

(a) forming a non-conducting coating on a plane surface of a first portion of a semiconductor body of one conductivity type;

(b) removing a band of said coating to expose an area of said surface;

(c) diffusing an impurity into the first portion from said surface within the area to form a layer of the same conductivity type as the first portion, the layer having sufficient impurity concentration to prevent said surface within the area from inverting to the opposite conductivity type to said one conductivity type;

(d) reforming a non-conducting coating on said surface within the area;

(e) and diffusing an impurity into a hole opened through said coating to said surface to form a second portion of said opposite conductivity type defining a rectifying junction between the second portion and the remainder of the first portion, with said junction extending to said surface underneath said coating about the second portion, the boundary of said junction at said

surface being completely surrounded by the layer.

26. A method for making a semiconductor diode comprising the steps of:

(a) forming a non-conducting coating on a plane surface of a semiconductor body of one conductivity type;

(b) removing a band of said coating to expose an area of said surface;

(c) diffusing an impurity into said body from said surface within the area to form a layer of the same conductivity type as said body, the layer having sufficient impurity concentration to prevent said surface within the area from inverting to the opposite conductivity type to said one conductivity type,

(d) reforming a non-conducting coating on said surface within the area;

(e) diffusing an impurity into a hole opened through said coating to said surface to form a layer of said opposite conductivity type defining a rectifying junction between said last mentioned layer and the remainder of said body, with said junction extending to said surface underneath said coating about said last mentioned layer, the boundary of said junction at said surface being completely surrounded by said first mentioned layer;

(f) and attaching ohmic contacts to said layers.

27. A method as defined in claim 26 wherein the area and said first mentioned layer extend to the periphery of said body.

28. A method as defined in claim 26 including the further steps of reforming a non-conducting coating on said last mentioned layer within said hole, one ohmic contact being attached to said last mentioned layer through a hole opened through said reformed coating to said surface, and the other ohmic contact being attached to said first mentioned layer through a hole opened through the non-conducting coating on said surface within the area, said first mentioned layer having its innermost edge lying inside said other contact.

29. A method for making a transistor comprising the steps of:

(a) forming a non-conducting coating on a plane surface of a semiconductor body of one conductivity type;

(b) diffusing an impurity into a hole opened through said coating to said surface to form a base portion of opposite conductivity type to said one conductivity type defining a base-collector junction between the base portion and the remainder of said body, with the base-collector junction extending to said surface underneath said coating about the base portion;

(c) reforming a non-conducting coating on said surfac within said hole;

(d) pening a smaller hol through said last mentioned c ating t said surfa e, and removing a band of

said coating to expose an area of said surface completely surrounding the boundary of the base - collector junction at said surface;

(e) and diffusing into said smaller hole and into the area an impurity to form an emitter portion of said one conductivity type defining an emitter-base junction between the emitter portion and the remainder of the base portion, with the emitter-base junction extending to said surface underneath said coating about the emitter portion, and a further portion of said one conductivity type, the further portion having sufficient impurity concentration of said one conductivity type to prevent said surface within the area from inverting to said opposite conductivity type;

(f) and attaching emitter base and collector contacts to the emitter portion, base portion and said body respectively.

30. A method as defined in claim 29 wherein the area and the further portion extend to the periphery of said body.

31. A method as defined in claim 29 including the further steps of reforming a non-conducting coating on said surface within said smaller hole and within the area, the emitter contact being attached to the emitter portion through a hole opened through said last mentioned coating to said surface inside the emitter-base junction, the collector contact being attached to said body through a hole opened through said last mentioned coating to said surface within the area, the further portion having its

innermost edge lying inside the collector contact, and the base contact being attached to the base portion through a hole opened through the coating covering the base portion to said surface inside the base-collector junction.

32. A method for making a transistor comprising the steps of:

(a) forming a non-conducting coating on a plane surface of a semiconductor body of one conductivity type;

(b) diffusing an impurity into a hole opened through said coating to said surface to form a base portion of opposite conductivity type to said one conductivity type defining a base-collector junction between the base portion and the remainder of said body, with the base-collector junction extending to said surface underneath said coating about the base portion;

(c) reforming a non-conducting coating on said surface within said hole;

(d) diffusing an impurity into a smaller hole opened through said last mentioned coating to said surface to form an emitter portion of said one conductivity type defining an emitter-base junction between the emitter portion and the remainder of the base portion, with the emitter-base junction extending to said surface underneath said coating about the emitter portion;

(e) reforming a non-conducting coating on said surface within said small hole;

(f) removing a band of said coating to expose an area of said surface within the base portion completely surrounding the boundary of the emitter-base junction at said surface;

(g) and diffusing an impurity into the area to form a further portion of opposite conductivity to said one conductivity type, the further portion having sufficient impurity concentration to prevent said surface within the area from inverting to said one conductivity type;

(h) and attaching emitter, base and collector contacts to the emitter portion, base portion and said body respectively.

33. A method as defined in claim 32 wherein the emitter contact is attached to the emitter portion through a hole opened through said last mentioned coating, and including the further steps of reforming a non-conducting coating on said surface within the area, and attaching the base contact into a hole opened through such reformed coating to said surface within the area, the further portion having its innermost edge lying inside and its outermost edge lying outside the base contact.

*

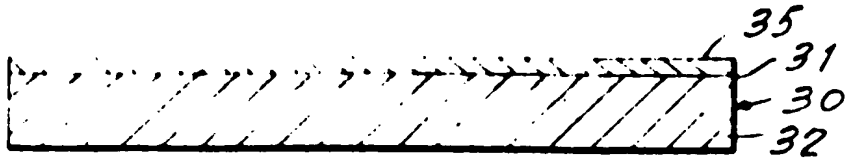


Fig. 1

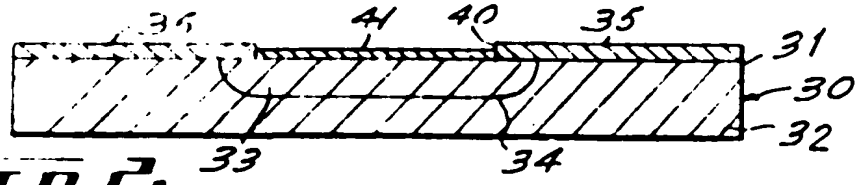


Fig. 2

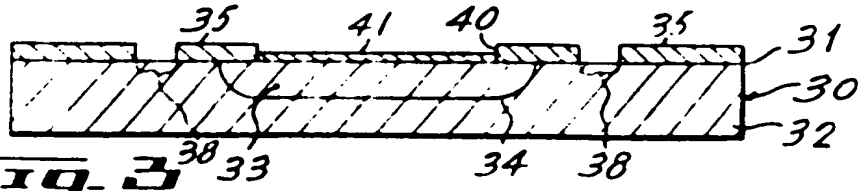


Fig. 3

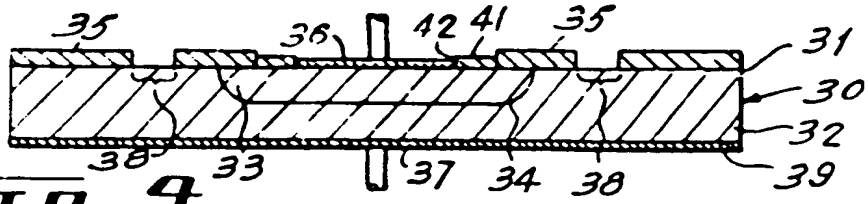


Fig. 4

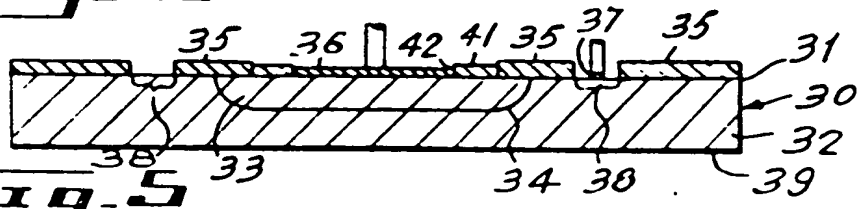


Fig. 5

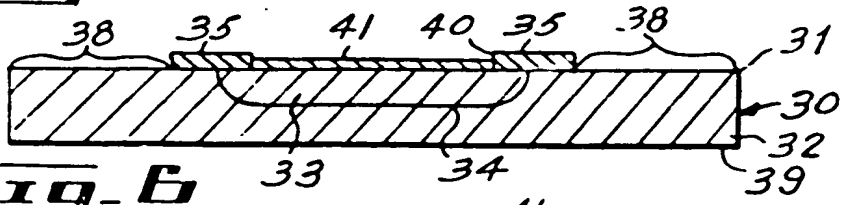


Fig. 6

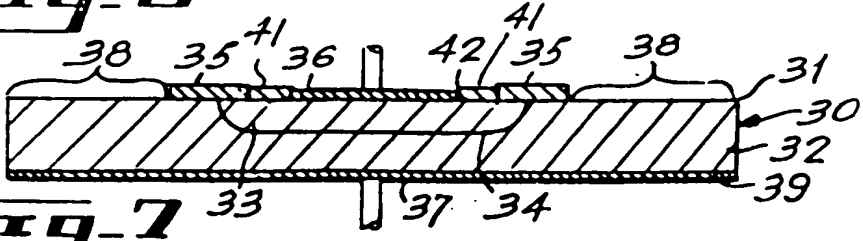


Fig. 7

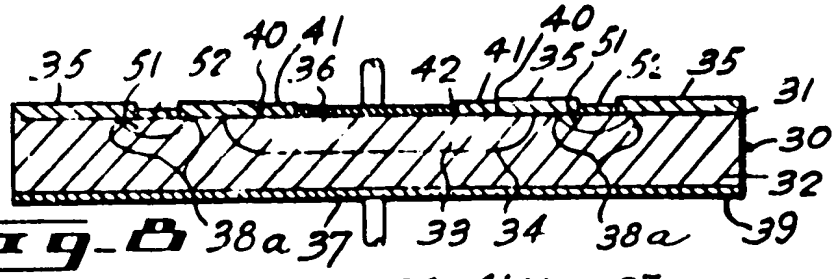


Fig-8

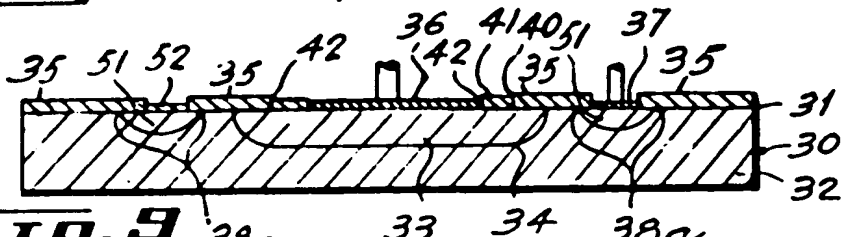
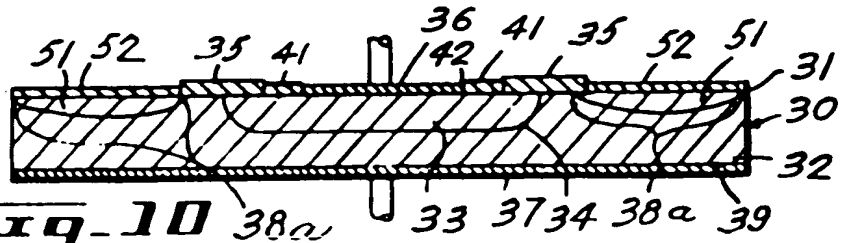


Fig-9



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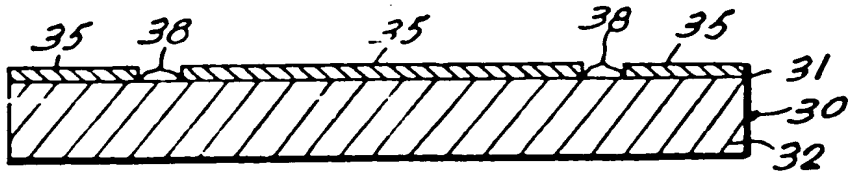

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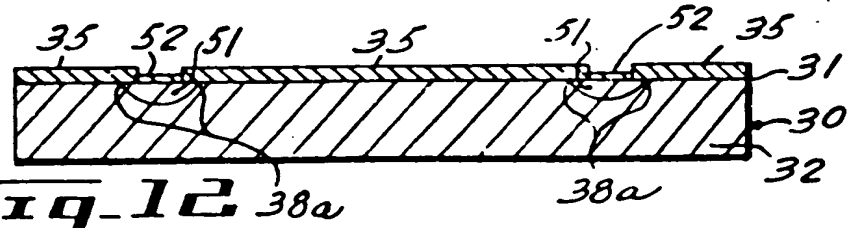


Fig-12

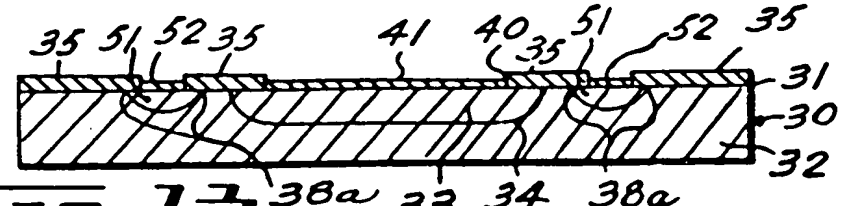
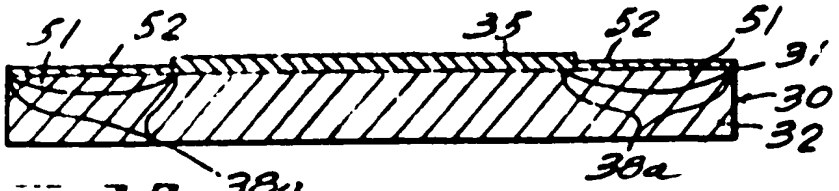


Fig-13



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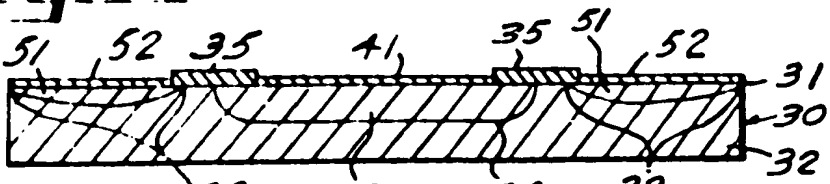

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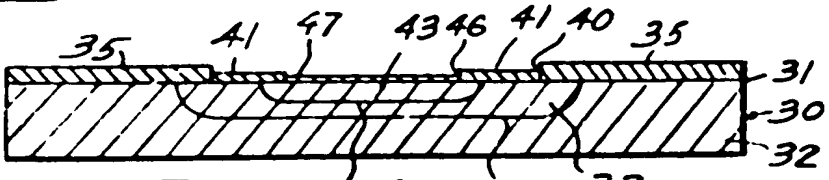

Fig-16

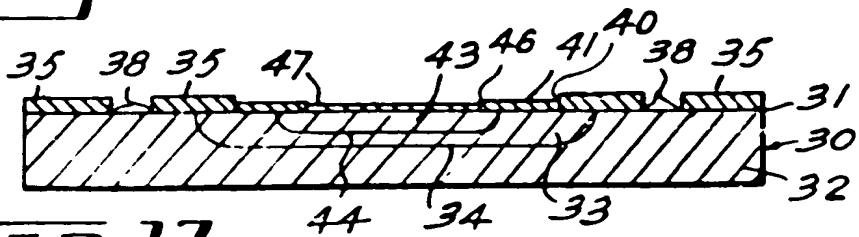

Fig-17

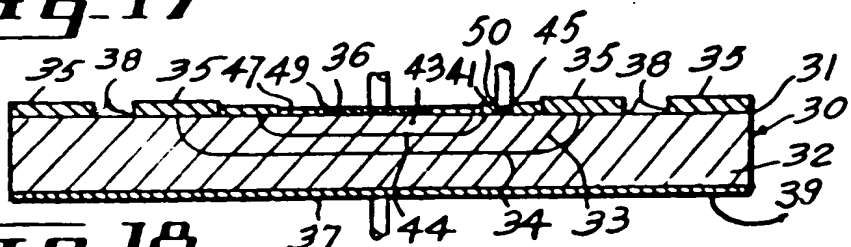

Fig-18

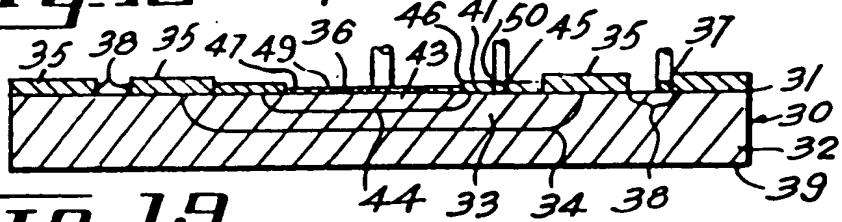

Fig-19

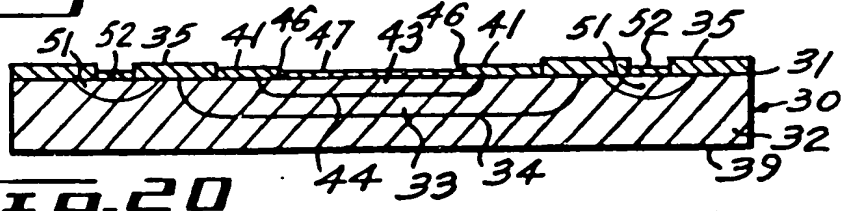

Fig-20

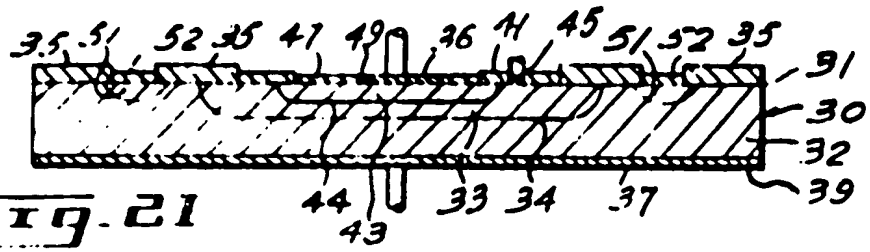

Fig. 21

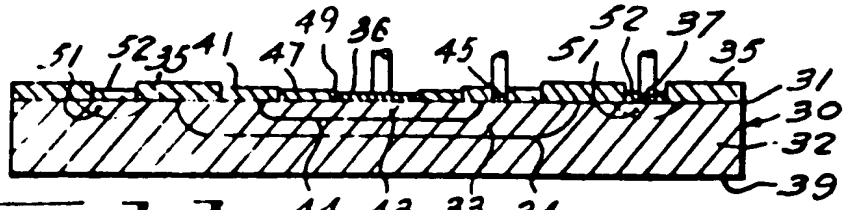

Fig. 22

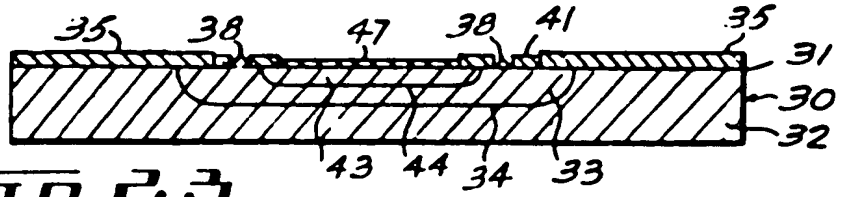

Fig. 23

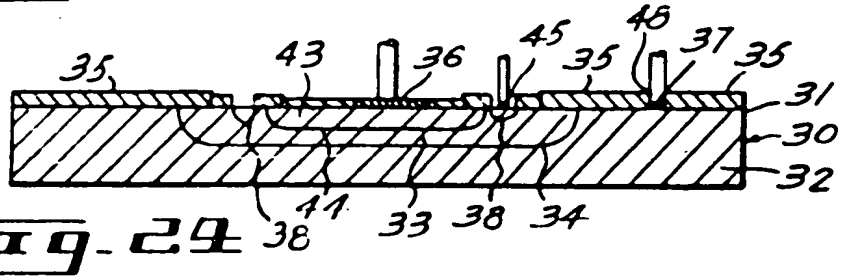

Fig. 24

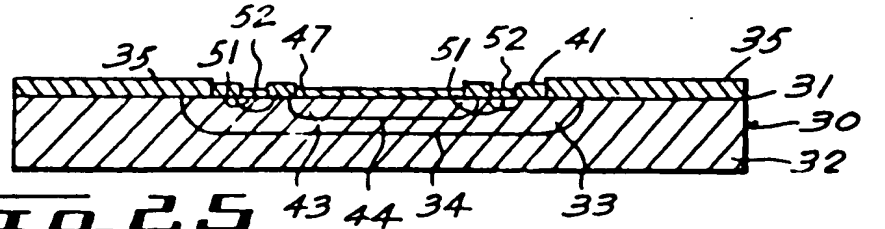

Fig. 25

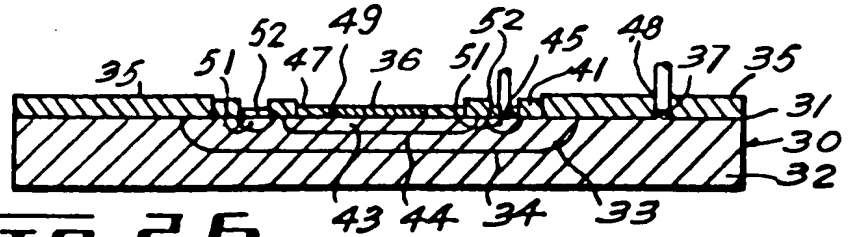

Fig. 26